An 'ultra-fidelity' MOSFET power amplifier module

David Tilbrook

The demands of the 'digital era' require power amplifiers of unparallelled performance in every critical aspect – power output, total harmonic distortion, dynamic distortion, stability, and subjective 'sound' (or lack of it, in reality). It is no easy matter to meet, let alone exceed, the criteria required, but we believe this amplifier does just that. Two of these modules will be employed in our upcoming ultra-fidelity stereo power amplifier, the companion to our popular preamp published earlier.

Part 1

THIS PROJECT represents the second in our series of ultra-fidelity audio components. The first was the AEM6010 Ultra-fidelity Preamplifier which was designed as a no-compromise unit with subjective performance being the most important design criterion. This is the approach taken in the AEM6000 power amplifier. Its objective performance, such as the total harmonic distortion (THD), frequency response, slew rate and stability is excellent, but the vast majority of development time has been spent on achieving the best possible subjective performance. The design uses MOSFET output transistors with what has become known as a fully symmetric voltage amplifier stage driven by an asymmetric cascade differential pair which employs both bipolar transistors and a dual-JFET. This overall circuit topology was selected only after a great deal of experimentation and was found to give the best subjective performance of the various topologies tried during development. The design does not use an excessive amount of overall feedback and this, combined with intrinsic high speed, yields an amplifier with superb stability characteristics.

Output stage considerations

In order to understand the reasons for the choice of this particular topology it is useful to start at the output stage and work backwards. The output stage employs two pairs of Hitachi complementary power MOSFETs, the n-channel 2SK176 and p-channel 2SJ56. These are higher power dissipation and higher voltage versions of the 2SK134/2SJ49s used in the AEM6500 general purpose power amp modules (July '86 issue). The main limitation of these earlier MOSFETs that prevents their use in this application is their relatively low maximum drain-to-source voltage rating of 140 volts. In other words, the maximum voltage at any instant that can be applied from the drain to the source of these MOSFETs must never exceed 140 volts, otherwise permanent damage to them may occur.

The power MOSFET is a particularly robust device but it can be damaged by excessive voltage and so it is very important that this criteria be well controlled. Since this power amplifier, like most modern power amplifier designs, is intended to be powered from a rectified and filtered but unregulated power supply, the supply voltage varies proportionally with the mains voltage. Although the mains voltage is rated nominally at 240 volts it varies about this figure, sometimes very considerably. The mains voltage at our laboratory in Wahroonga in Sydney, for example, lies somewhere between 245 and 255 volts depending on the time of day. We have been advised by various electricity councils in several states that a maximum mains supply voltage of around 265 volts should be allowed for.

If, for example, a 300 VA 47-0-47 V power transformer was to be used for the power supply of a power amplifier then the supply voltage after full-wave rectification and with a load of 300 watts, would be around ± 66.5 volts. Under "no-load" conditions, supply voltages would be approximately 5% higher than this at around ± 70 volts. This is the case for a mains supply voltage of 240 volts and you need to allow for a peak mains supply of around 265 volts. Under these circumstances, the power supply rails could be as high as ± 77 volts. If this power supply were now used in conjunction with an output stage employing 2SK139/2SJ49 power MOSFETs then it is possible for the maximum drain-to-source voltage of 140 volts to be exceeded.

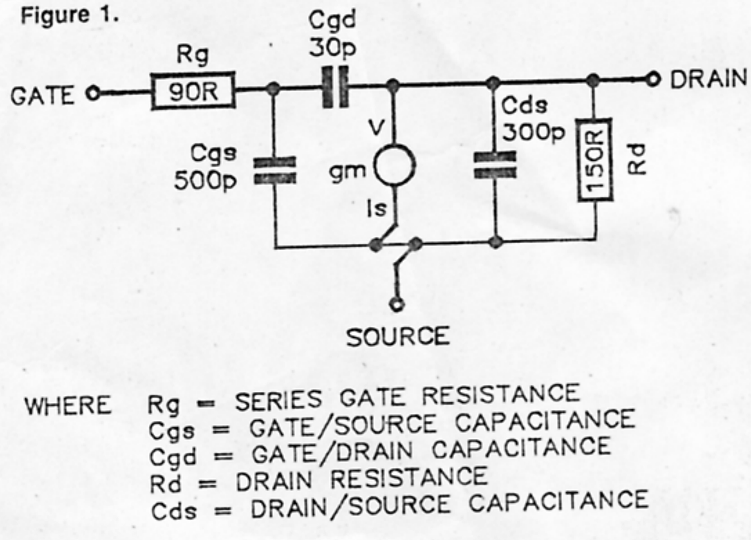
The vast majority of modern solid state power amplifier output stages operate in what is referred to as "class B" at high output powers. This means that only one side of the output stage is operational during any half cycle of the output signal waveform, the complementary side being 'off'. The complementary output devices alternate passing control of the load to and from each other each time the output signal voltage crosses zero. At full power then, even during a short, very large transient signal voltage, one set of output devices will be hard on, showing minimum drain-to-source resistance (as I'm talking about MOSFETs here) and allowing the output to approach as closely as possible to one or other of the two supply rails. Under this condition almost the full supply voltage is applied to the devices which are off during that half cycle. There is some voltage drop across the 'on' MOSFETs due to their source-to-drain resistance and their source resistors. Even this, however, cannot be relied upon because the module might be operated with no load and hence these drops will not be present. Under these conditions it is quite possible to apply in excess of 150 volts across those MOSFETs in the 'off' state. Under such circumstances, power MOSFETs with a maximum drain-to-source voltage of 140 volts can be relied upon to have a very short life indeed!

For these reasons I have chosen the 2SK176/2SJ56 complementary pair for use in this design. These devices are even more robust than their counterparts. They have a maximum drain-to-source supply voltage rating of 200 volts, maximum power dissipation rating of 125 watts and a maximum drain current rating of 8 amps. The use of two pairs of these devices in the output stage of this power amplifier makes it appropriate for use with supply voltages ranging from ± 50 to ± 70 volts, allowing maximum output powers from around 100 to over 200 watts RMS. If you were building a power amplifier to accompany a compact disk player and perhaps a modern pair of direct radiating loudspeakers, then you should opt for the higher power.

The power MOSFET is a voltage driven device. By this I mean that the applied voltage expressed between its gate and its source determines the resistance of the device from its drain to its source. If the gate-to-source voltage is increased the drain-to-source resistance is decreased (n.b: This is only the case with enhancement mode devices, most JFET devices, for example, are depletion mode types and operate more like a vacuum tube. Increasing gate voltage causes an increasing drain-to-source resistance). The maximum gate-to-source voltage that can be applied is a characteristic of the particular choice of MOSFETs employed. If the maximum gate-to-source voltage of the power MOSFETs is exceeded by the driving amplifier stages, the MOSFETs will be damaged irreparably. This is the most common reason for MOSFETs to be destroyed once they are properly in circuit (that is, not from electrostatic discharge) and to prevent this possibility a series diode/zener diode string is incorporated in parallel with the MOSFET from gate to source. The zener diodes specified are 12 V/1 W types and, being in series with the diodes, prevent the gate-to-source voltage from exceeding 12.6 volts.

The circuit diagram in Figure (1) shows the equivalent circuit of a power MOSFET similar to the types employed in this design.

Figure 1.



Equivalent circuit of a typical power MOSFET

The gate appears as a 90 ohm resistance in series with a 30 pF capacitance to the drain and a 500 pF capacitance to the source. At dc, the input resistance is many thousands of megohms, being determined by the effective dielectric constants of these two input capacitances. The amount of gate-to-source capacitance for the n-channel and p-channel power MOSFETs is substantially different, with the capacitance usually being substantially less for the n-channel types.

The equivalent circuit gives us several insights into the characteristics of these power MOSFETs. At low frequencies the gate impedance is extremely high. As the frequency increases, however, the gate-to-source and gate-to-drain capacitances become increasingly important, decreasing the input impedance substantially. When used in a class B amplifier the different load capacitance that is presented by the n-channel and p-channel MOSFETs produces an asymmetric load to the drive stage at high frequencies and, if uncorrected (a common omission in published designs), this tends to increase high frequency second harmonic distortion. Fortunately, the problem is realatively simply solved by increasing the gate-to-source capacitance of the n-channel power MOSFETs by the addition of parallel 330 pF capacitors connected between the gate and source.

The equivalent circuit also gives us an insight into the high frequency performance of the power MOSFET. The effective gate resistance and the gate-to-source capacitance couple to form a low-pass first-order filter that determines the high-frequency response of the device. The cutoff frequency of a power MOSFET is well in excess of 3 MHz when correctly driven and the absence of an effect called "minority carrier storage" ensures that the power MOSFET is unrivalled in switching speed. The extremely fast response, coupled with the high input impedance and the gate-to-source and gate-to-drain capacitances, however, make the devices prone to oscillation if they are incorrectly used. The cure is to decrease the cutoff frequency of the output stage by the addition of series gate resistors for each device. These add to the internal gate resistance and decrease the frequency response of the output stage. These resistors, shown in the AEM6000 main circuit diagram as 270 ohms, must be mounted physically as closely as possible to the gates of the power MOSFETs. Remember that these components are incorporated to cure a problem that will only exist at high frequencies, so any inductance in series with the gate circuitry will decrease their effectiveness. Although these series resistors do decrease the slew rate of the output stage slightly, the effect is not dramatic and the overall slew rate figures of the power amplifier remain very good. The extremely high slew rate of the output stage facilitates a very broad open-loop bandwidth which in turn contributes greatly to the reduction in slew-induced and other dymanic distortion mechanisms.

Power amplifiers employing the more conventional bipolar output transistors often suffer from inferior open-loop bandwidth and tend to rely on the application of negative feedback to linearise high frequency performance. In this case, the amount of overall negative feedback decreases with increasing frequency, leading to increased distortion figures at higher frequencies.

There are other advantages of the power MOSFET that are not revealed by examination of the equivalent circuit. Probably the most important of these is its thermal characteristics. The power MOSFET, unlike the bipolar transistor, has a negative temperature coefficient when operating above a certain drain current. In the case of the 2SK176 and 2SJ56 ▶

devices, this is around 100 mA. Above this operating current the power MOSFET has the characteristic such that an *increase* in its operating temperature will cause a *decrease* in the drain-to-source current for a given gate-to-source voltage. The positive temperature coefficient exhibited by the bipolar transistor, on the other hand, causes an increase collector-to-emitter current as temperature rises when the base current is held constant. The increased collector-to-emitter current increases power dissipation within the device and the consequent increase in the operating temperature leads to a further increase in the collector-emitter current. The result is an effect called "thermal runaway" which leads inevitably to the to the destruction of the device. The negative temperature coefficient of the power MOSFET is the characteristic that makes it so robust in comparison to bipolar power transistors.

Inspection of the main circuit diagram of the AEM6000 power amplifier reveals that, associated with each output MOSFET there is a 0.22 ohm (0R22) resistor in series with the source. These resistors have a three-fold purpose. Firstly, they encourage current sharing between the two pairs of MOSFETs. This is particularly important if the devices are operated with a quiescent current of less than 100 mA. Secondly, they greatly improve the stability characteristics of the output stage, and finally, they help to linearise the transfer characteristics of the devices. The final components used to ensure stability of the output stage are associated with the RC network connected from the output of the power amplifier to ground, which serves to provide the power MOSFETs with a load at high frequencies. At a sufficiently high frequency, the two 22 ohm/1 watt resistors in parallel represent an 11 ohm load from output to ground.

The initial specification for the AEM6000 power amp was that it should be capable of delivering in excess of 200 watts RMS into an 8 ohm load. This means that, when driven by a sinewave it will develop 40 volt RMS across the load (i.e: one having a peak amplitude of 56.6 volts). Since the minimum drain-to-source on-resistance for the Hitachi devices is around 1.8 ohms, I would expect a voltage drop of around 6 volts as a result of the current necessary to develop 200 watts in an 8 ohm load. Allowing for a further voltage drop of around 1 volt across the source resistors, the required supply voltage to ensure 200 watts into an 8 ohm load would be around 64 volts. The recommended maximum suply voltage of around 70 volts should therefore suffice.

The voltage amplifier

The main voltage amplifier is a two-stage fully symmetric differential amplifier. The differential voltage amplifier circuit was chosen since it was determined that the open-loop distortion should be kept to a minimum. By this I mean that the distortion of each individual amplifier stage within the power amplier should be a minimum. In this way, good overall distortion performance can be achieved without the introduction of large amounts of overall negative feedback. The differential amplifier has a much lower intrinsic distortion than a single-ended voltage amplifier. This is shown clearly by the diagram in Figure 2. This graph shows the difference in distortion performance between a differential pair and a single transistor for various open-loop gains. The distortion figures for the differential pair are around 30 dB below those of a single transistor.

The voltage gain stage is fully symmetric since it became clear during the development of this power amplifier that the subjective performance of this type of voltage amplifier is clearly superior to the earlier asymmetric designs.

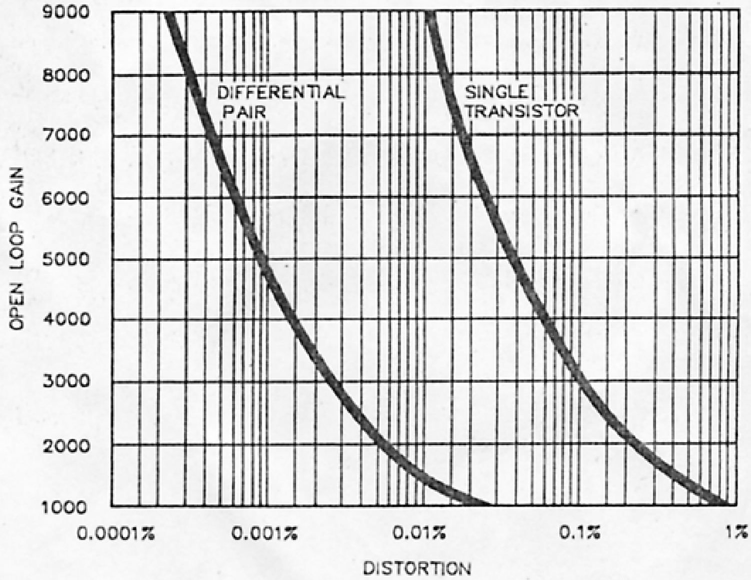


Figure 2.

However, this was found only to be the case in those parts of the power amplifier design that necessitated large signal level, and hence large signal slopes or slew rate (the ability to change voltage output very rapidly). In fact, both the subjective and objective performance of fully symmetric differential pairs employing bipolar transistors proved to be inferior to that of an asymmetric differential pair when used at low signal levels.

The voltage amplifier stage consists of the fully symmetric differential pairs formed by Q11-Q14, followed by a differential voltage amplifier stage formed by Q15-Q18 and fed from a pair of constant-current sources formed by Q9, Q10 and their associated resistors and diodes.

The input differential pair

The input stage is an asymmetric cascade differential pair formed by the combination of a dual-JFET, Q1 and Q2, and a pair of bipolar transistors, Q3 and Q4. The correct operating conditions are established by two constant-current sources in conjunction with a zener diode. The first of these current sources is formed from Q7 and Q8 in association with resistors R13 and R14, while the second is formed from Q5 and Q6 and resistors R8 and R10.

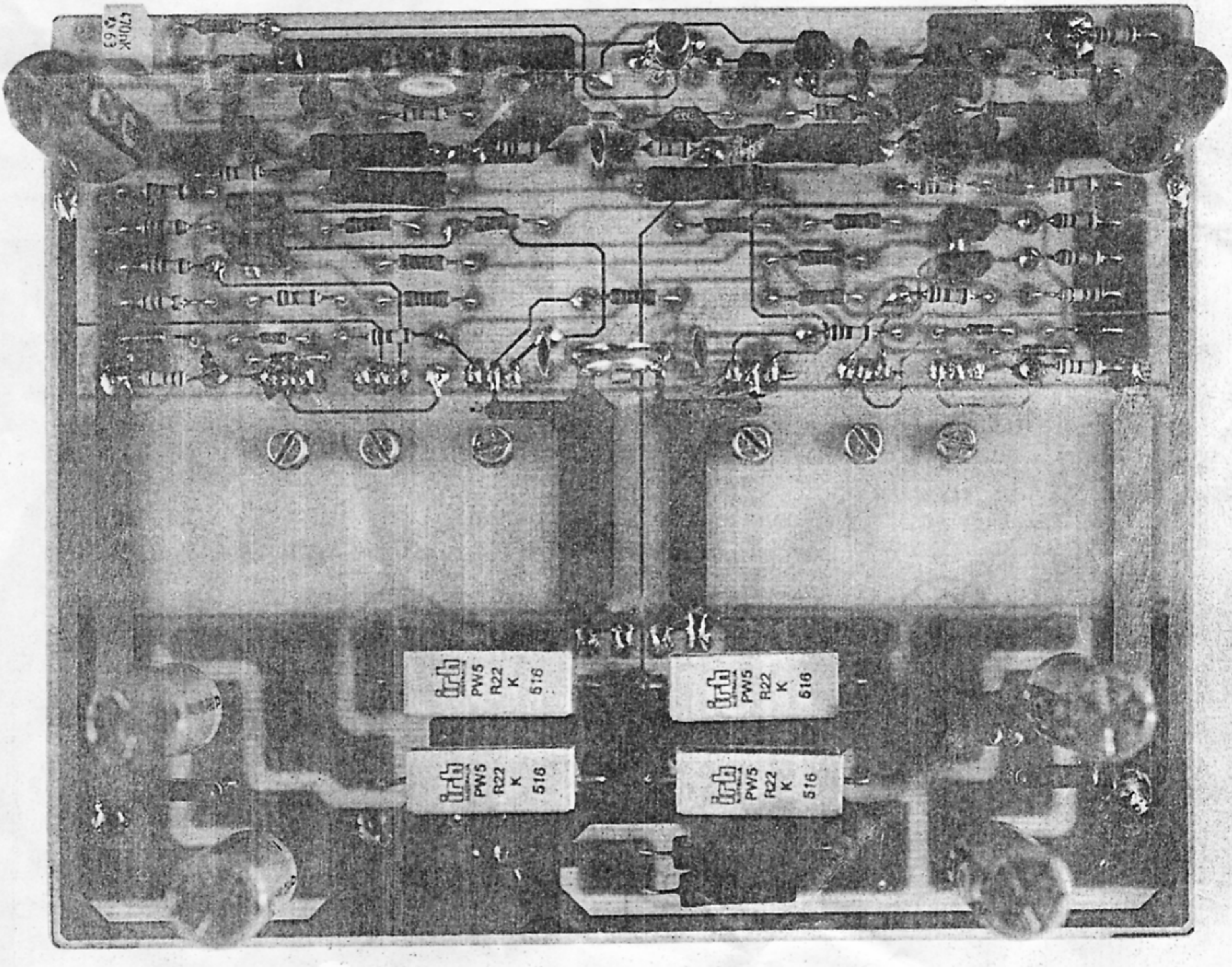
I have chosen an asymmetric input differential pair in preference to a fully symmetric stage since, as mentioned above, both the subjective and objective performance of the asymmetric circuit proved to be superior. The reasons for this are associated with a fundamental problem of symmetric stages, that of asymmetry of the characteristics of npn and pnp transistors. The reality is that, although the principle of a symmetric amplifier circuit is to oppose every npn device with a pnp device so that the non-linearities generated by these two devices cancel; in practise this does not occur. Because npn and pnp bipolar transistors have different characteristics, some asymmetry in the operation of the circuit is inevitable. This problem is most significant for small signal levels and so the choice of a fully symmetric stage using bipolar transistors for the input differential pair is, in my opinion, inappropriate. No doubt these remarks will cause some controversy, but my opinion is supported by both objective and subjective analysis of a variety of test amplifiers. Some of these were fitted with asymmetric stages. The test amps were otherwise identical. The CMRR (common mode rejection ratio) of the asymmetric stages was consistently superior to those of the fully symmetric stages as was the THD and the overall output offset voltage. The symmetric stages do exhibit decided advantages, however, for application in the voltage amplifier stages where the relatively poor CMRR performance is unimportant.

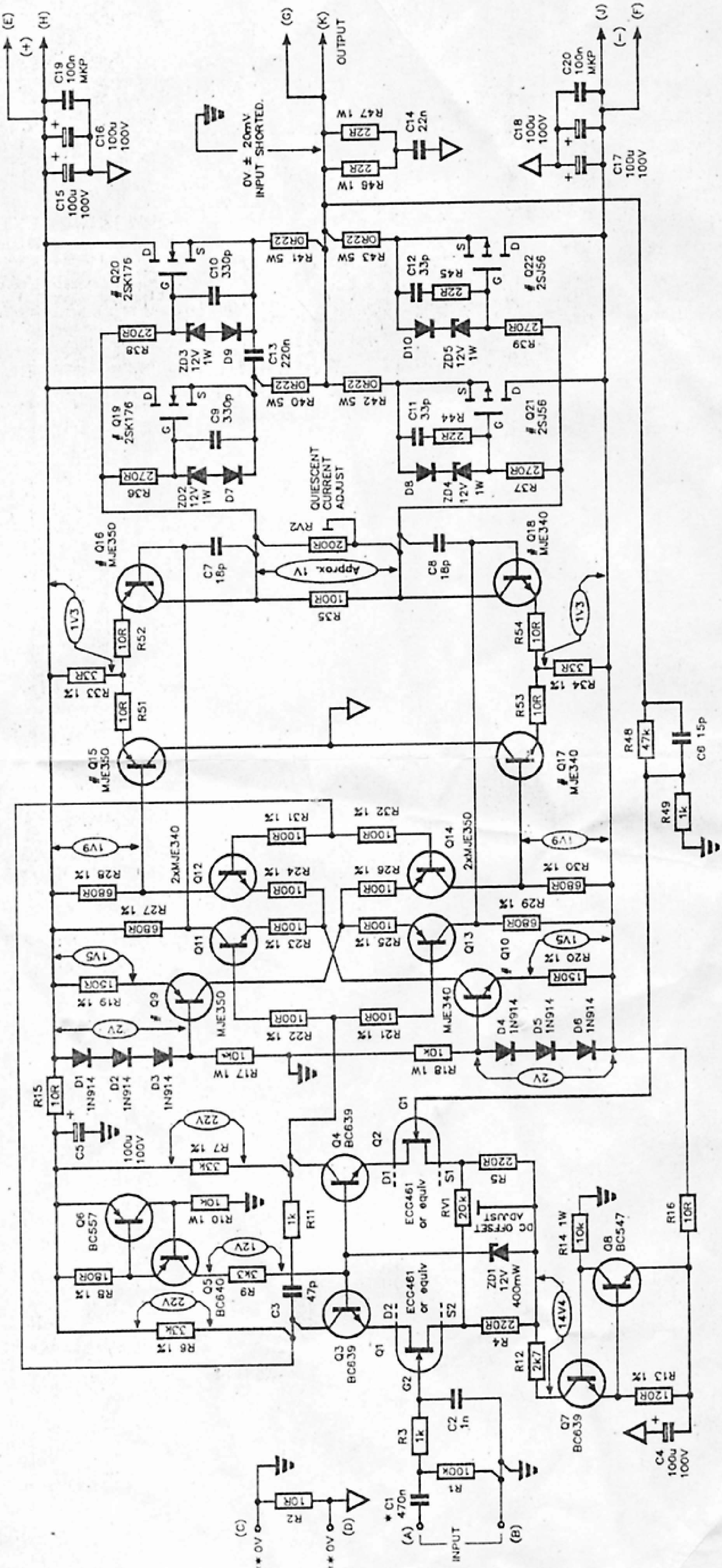
Another aspect of the input stage design that was found to be of particular importance to the subjective performance of the power amp, was the elimination of capacitors from the signal path. In particular, the dc blocking capacitor usually employed in the feedback loop to reduce the overall dc gain of the amp, and hence the dc offset, was found to cause significant degradation of subjective performance. In order to facilitate removal of this capacitor altogether, the dual-JFET input pair was required. If a bipolar transistor pair was to be used instead, the base-emitter bias current necessary would produce an input offset voltage of around 20 mV. After amplification by the dc gain of the power amp, an output offset voltage of around 1 V could easily result. The JFETS, of course, do not suffer from this problem. Furthermore, since the two JFETS are mounted on the same chip, this ensures excellent thermal tracking and consequent stability of the output offset voltage with temperature changes.

The power amplifier can be operated entirely direct-coupled if required, although some caution should be executed if attempting to do so. Remember that the power amp will be driven to full power from a 1 V input signal. Application of just 1 Vdc to the input of the power amp will result in full power dc signal (around 70 Vdc) being applied to the base driver of your loudspeakers with obvious catastrophic results! In next month's issue we will be describing a dc protection circuit that detects the presence of dc on the output stage of any power amp and automatically disconnects the loudspeakers if necessary. This unit will also be incorporated into the AEM6000 power amplifier and is recommended for use with this power amp module. In general, I would recommend the use of the input coupling capacitor C1. It has little, if any, effect on the subjective performance and could help to prevent a costly accident in the event of a dc offset problem associated with the preamplifier used to drive the power amp.

Next month I will be describing the construction of the power amp modules in detail and, as mentioned above, the design and construction of the dc protection circuitry. Until then, take the time to examine how the circuit functions, as described in the Circuit Operation section of this article. Direct- (or dc-) coupled power amps, particularly high power ones, can be difficult to service at times and familiarity with the circuit under these circumstances is imperitive. ▶

Below: A prototype board.





N.B. These two earths must remain separated on the p.c.board
Run separate wires to them from the power supply
filter capacitors. This will be explained in greater detail in part 2.

NOISY EARTH

CLEAN EARTH

VOLTAGES
Expected approximate voltages with the input shorted (connect (A) to (B))
-refer to circuit operation

* C1 IS OPTIONAL (see text)

** JOIN TOGETHER ONLY AT POWER SUPPLY

Q1,Q2 .....ECG461 IS A DUAL JFET BY NEW-TONE ELECTRONICS (NTE) OR A SUITABLE EQUIVALENT (see text)

MOUNTED ON HEATSINK

D7-D10 ARE 100V 1A FAST RECOVERY DIODES

CIRCUIT OPERATION

The input signal is coupled via capacitor C1 to resistors R1 and R3. This capacitor provides dc decoupling, preventing any dc component of the input signal from being connected to the input of the power amp. With the exception of this capacitor, the entire power amplifier is dc coupled, so the gain of the circuit at dc is the same as that for signals within the audio passband. i.e: around 48 with the feedback components specified. This will be covered in greater detail later, but it implies that the application of 1 Vdc to the input without the dc blocking capacitor installed, would result in roughly 48 Vdc appearing at the output of the power amp and hence to the bass driver of any loudspeaker system connected. This, of course, would result in very rapid destruction of the bass driver. The use of C1 therefore, although still optional, is highly recommended.

Resistor R3 and capacitor C2 form a low-pass first-order RC filter, the purpose of which is to limit the maximum signal slope of the input signal. If it is assumed that the output impedance of the preamp used in conjunction with the power amp is significantly less than the value of R3 (1k), then the –3 dB point for this filter is given by the simple equation:

$$f = 1/(2\pi RC)$$

where f is the –3 dB point
R is the resistance of R3
C is the capacitance of C2.

i.e: $f = 1/2(\times 10^3 \times 10^{-9})$
$= 159$ kHz.

This frequency clearly lies well above the audio passband and therefore has no effect on the frequency response performance of the power amp. Its purpose, as mentioned above, is to limit the maximum signal slope of the input signal. This is necessary to help to ensure complete freedom from slew induced distortion, sometimes referred to as TIM, or transient intermodulation distortion. This type of distortion is analogous to a more commonly understood distortion mechanism, that of clipping. In the case of clipping, distortion is generated when the input signal drives the power amp output beyond the limits of its available supply voltage. In a similar manner, if you attempt to drive the power amp beyond its maximum slew rate, the signal 'clips' or 'hard limits' and gross distortion results with products spreading across the audio spectrum. The solution is to design an amplifier with excellent slew rate figures and then to limit the maximum signal slope by the use of simple high frequency low-pass filter so that the slew rate limit of the design cannot be approached.

The effectiveness of this approach is, to a certain extent, dependent on the quality of the input filter. It is important to ensure that the filter employed introduces minimum signal degradation of its own. It is for this reason that the simple first-order RC is used which seems to introduce negligable, if any, degradation of the subjective or objective performance, provided the right type of capacitor is employed. A ceramic capacitor, for example, should not be used in this application. Ideally, use a polypropylene capacitor if one is available or, alternatively, use a good quality MKT type metallised polyester capacitor. Polypropylene capacitors are, unfortunately, very difficult to obtain in Australia in small quantities and also tend to be expensive, but they exhibit clearly superior characteristics in audio signal applications in comparison to many other types. This is also true for the other capacitors in the power amp, not just the input capacitor, C1, but the two high-frequency power supply decoupling capacitors C19 and C20 as well.

Resistor R1 provides a dc reference for the gate of the first of the JFETs (Q1) which, in conjunction with Q2 (also a JFET), forms the input differential pair. Note that Q1 and Q2 are a dual-JFET contained within a single encapsulation, fabricated on the same substrate to ensure close thermal coupling. Its use is necessary since this power amplifier is entirely dc-coupled and as mentioned above, the gain of the amp at dc is the same as that for signals within the audio passband. If separate transistors are used, each device is free to 'float' at a different temperature (no matter how slight that may be) and a drifting dc offset will result. JFETs are used in preference to bipolar transistors since the JFET requires negligable bias current. If bipolar transistors were used the base-emitter current required produces a dc voltage drop across the bias resistor R1 which, after amplification by the dc voltage gain of the power amplifier, will produce significant levels of dc offset at the output.

The entire input stage actually consists of the dual-JFET described above, in combination with a cascade pair of bipolar transistors, Q3 and Q4. The operating conditions for the input stage are determined by a pair of constant-current sources and the zener diode ZD1. The first current source is formed from transistors Q7, Q8 and their associated resistors R13 and R14. At the moment power is applied to the circuit current flows from the clean earth via R14 through the base of Q7 to the base of Q8 and resistor R13. When the voltage developed across R13 reaches 0.64 V, transistor Q8 is biased on and current flowing through R14 is robbed from the base of Q7. The circuit stabilises so that the current flowing through R13 is such that the voltage across it will be around 0.64 V. This is true regardless of the actual value of resistor R13, so varying the value of this resistor enables the current through it to be varied. Furthermore, once the value of R13 has been chosen, the circuit maintains the current through it at a constant level and the circuit acts as a constant-current source, or actually a constant-current sink in this case. With the value of resistor R13 set at 120 ohms, the current sink will set the current flowing through resistor R12 to 0.64/120 = 5.3 mA.

Resistor R12 is included for two reasons. Firstly, it drops a constant voltage as a result of the constant current flowing through it to decrease the power dissipation in the current sink. Since the current is set by the constant-current sink at around 5.3 mA, a voltage drop of around

$$5.3 \times 10^{-3} \times 2.7 \times 10^{3} = 14.4 \text{ volts}$$

will be produced. Secondly, it acts to protect the input stage in the event of a failure of the constant-current sink.

The current set by the constant-current sink flows through the two cascade differential pairs Q1, Q3 and Q2, Q4 as well as through the zenor diode ZD1, which provides a dc reference for the bases of the cascade pair. In order to ensure that the differential pair is fed from a constant current to ensure maximization of the common mode rejection ratio (CMRR), it is necessary to use a second current source specifically for the zener diode. This current source is formed from transistors Q5, Q6 and their associated resistors R8 and R10. This constant-current source works in an analogous manner to that formed from Q7 and Q8 and establishes a current of 0.64/180, or around 3.6 mA. This current flows through the 33k resistor R9, which serves the same purpose as that of R12, and produces a voltage drop of around 11.9 volts. The current available to flow through the differential pair is the difference between the currents set by these two differential pairs, i.e.: around 1.18 mA. This current is shared equally between the two cascade differential stages so that a current of around 900 uA flows through the 33k resistors R6 and R7 producing a voltage drop across these of around 22 V.

The second stage is a fully symmetric differential amplifier employing the bipolar transistors Q11, Q12, Q13, Q14 and their associated resistors R21 to R32. The operating point for this stage is established by a pair of constant-current sources formed from Q9, Q10, R17-R20 and diodes D1-D6. The operation of this type of constant-current source can be understood by considering the negative current source first. The three diodes in series are biased on by current flowing through R18 from the clean earth to the negative rail. The current produces a voltage drop across each of approximately 0.7 V, giving a total voltage drop of 2 V. Since this is applied to the base of Q10, the voltage drop across resistor R20 is also constant giving rise to a constant current through it and hence through the emitter-collector junction of Q10. Since the voltage applied to the base of Q10 is 2 V, around 1.5 volts will be applied across resistor R20, giving rise to a current of 1.5/270 = 5.6 mA.

The current delivered by the constant current sources to the differential voltage amplifier is shared equally between the load resistors R27 and R28, producing a voltage drop across these resistors of around 1.9 V. This voltage biases the final and main voltage amplifier stage comprising Q15-Q18 and their associated resistors R33, R34, R51-R54 and capacitors C7 and C8. The application of 1.9 V to the bases of this stage causes a voltage of around 1.3 V to be expressed across resistors R33 and R34 and establishes the bias conditions for this stage. Since R33 and R34 are 33 ohms the current is set at 1.3/33 = 40 mA. This is a relatively large amount of operating current and is necessary to ensure that this stage has a sufficiently low output impedance to drive the input gate capacitance of the MOSFET final output stage. This helps to ensure very good open loop bandwidth which is essential for amplifier stability and freedom from slew induced distortion.

The final stage of the amplifier is the MOSFET current amplifier formed from the four power MOSFETs Q19-Q22 plus associated resistors and capacitors. The bias current for the output stage is set by adjustment of the preset potentiometer RV2. Since the current flowing through this preset is constant, the voltage dropped across it will be directly proportional to its resistance. As the voltage is incresed by increasing the resistance of the preset, the output MOSFET's are biased on and a quiescent current will flow from the positive rail to the negative rail through the MOSFETs. This is necessary to provide an area of class A operation to decrease crossover distortion and other nonlinearities that occur at low signal levels. Resistors R36-R39, in conjunction with the gate-to-source capacitance of the power MOSFETs, produce a low-pass first-order filter with a –3 dB point around 1 MHz which is necessary to ensure stability of the output stage. In addition, capacitor C13 acts to prevent oscillation that can occur because the two 2SK176s and the inductance of the source resistors R40 and R41 form a push-pull Colpitts oscillator circuit.

The source resistors have been included to linearise the transfer characteristics of the MOSFETs and also to assist current sharing between the two sets of MOSFETs. Some recently published designs employing power MOSFET output stages have omitted the source resistors, adopting the approach that the negative temperature coefficient of the MOSFETs makes these resistors unnecessary. The problem with this is that the MOSFETs' temperature coefficient is not constant and is a function of the source-drain current. Also, here the use of the source resistors in combination with the source-gate capacitors C9, C10, C13 and the RC networks R44, C11 and R45, C12 yields an output stage with maximum stability and long term reliability.

The RC network consisting of R46, R47 and C14 serves to ensure that the output stage has a load of high frequencies, again to ensure stability of the power amp output stage. Resistor R48 and R49, and capacitor C6, determine the gain of the power amp. The values shown set the overall voltage gain to 48 for frequencies within the audio passband. At higher frequencies the decreasing impedance of capacitor C6 applies an increasing amount of overall negative feedback, reducing the overall voltage gain.